

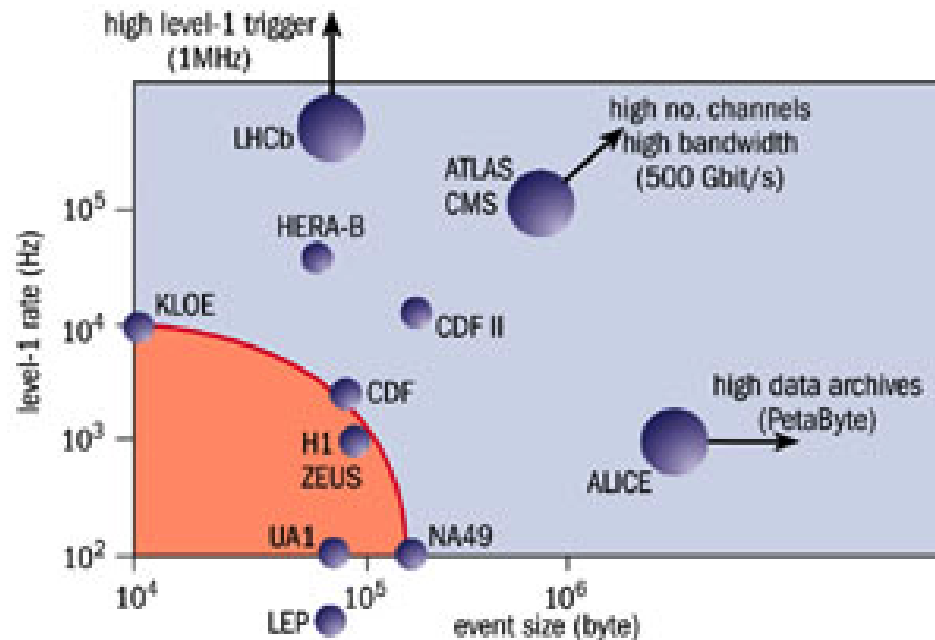
Next generation of Trigger/DAQ

Patrick Le Dû -



- Where are we today?
- Evolution 2005-2010
- On/off line boundaries
- What next ? 2010-2020
- LC's Triggers
- Technologies
- What about standards?
- Technology transfer to others fields

General comments about Trigger/DAQ



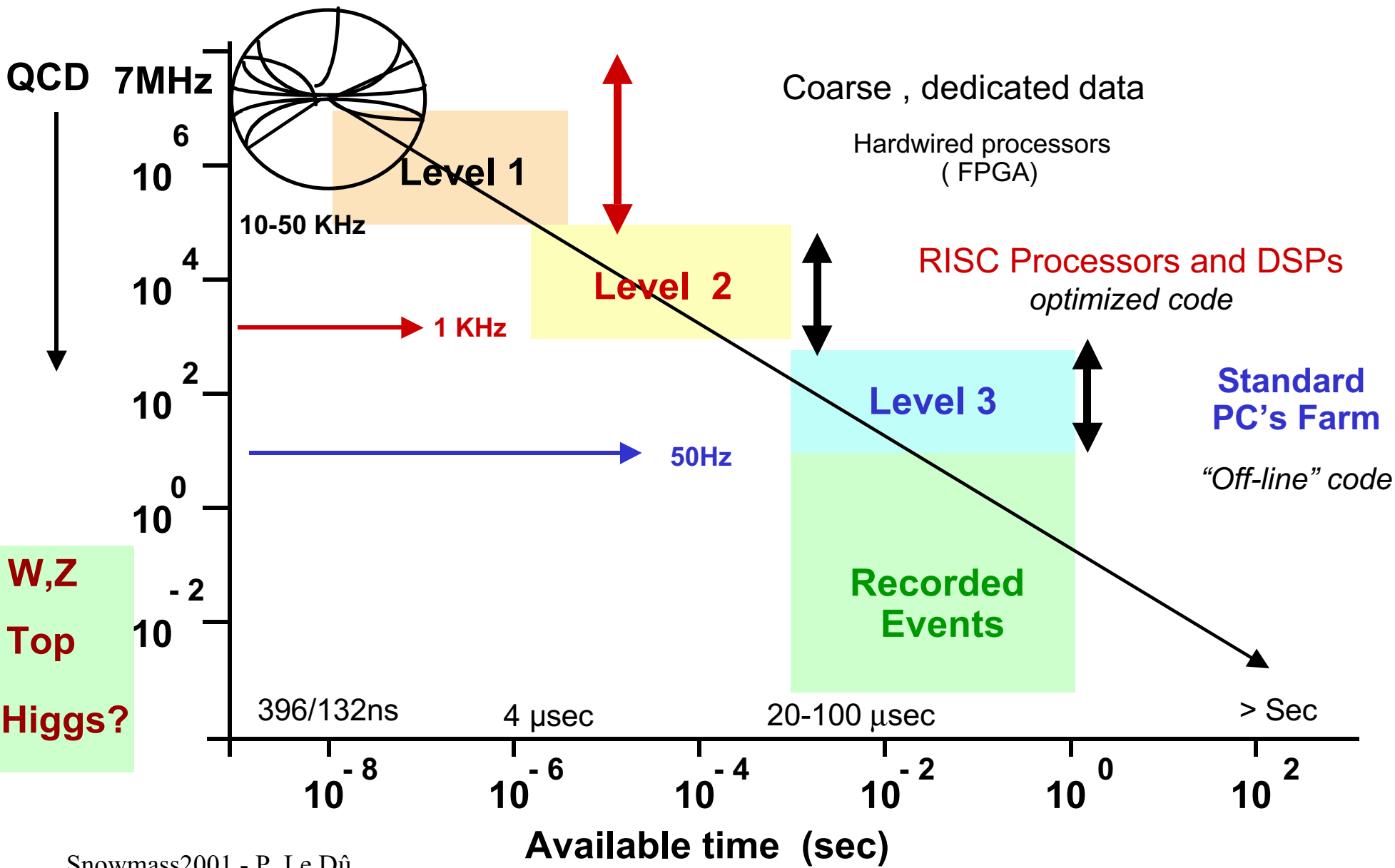
- From the Physics: NO loss
- From the Detector : Deadtimeless
- From the Machine : use 100%
- from T/DAQ people: maximum efficiency and minimum maintenance

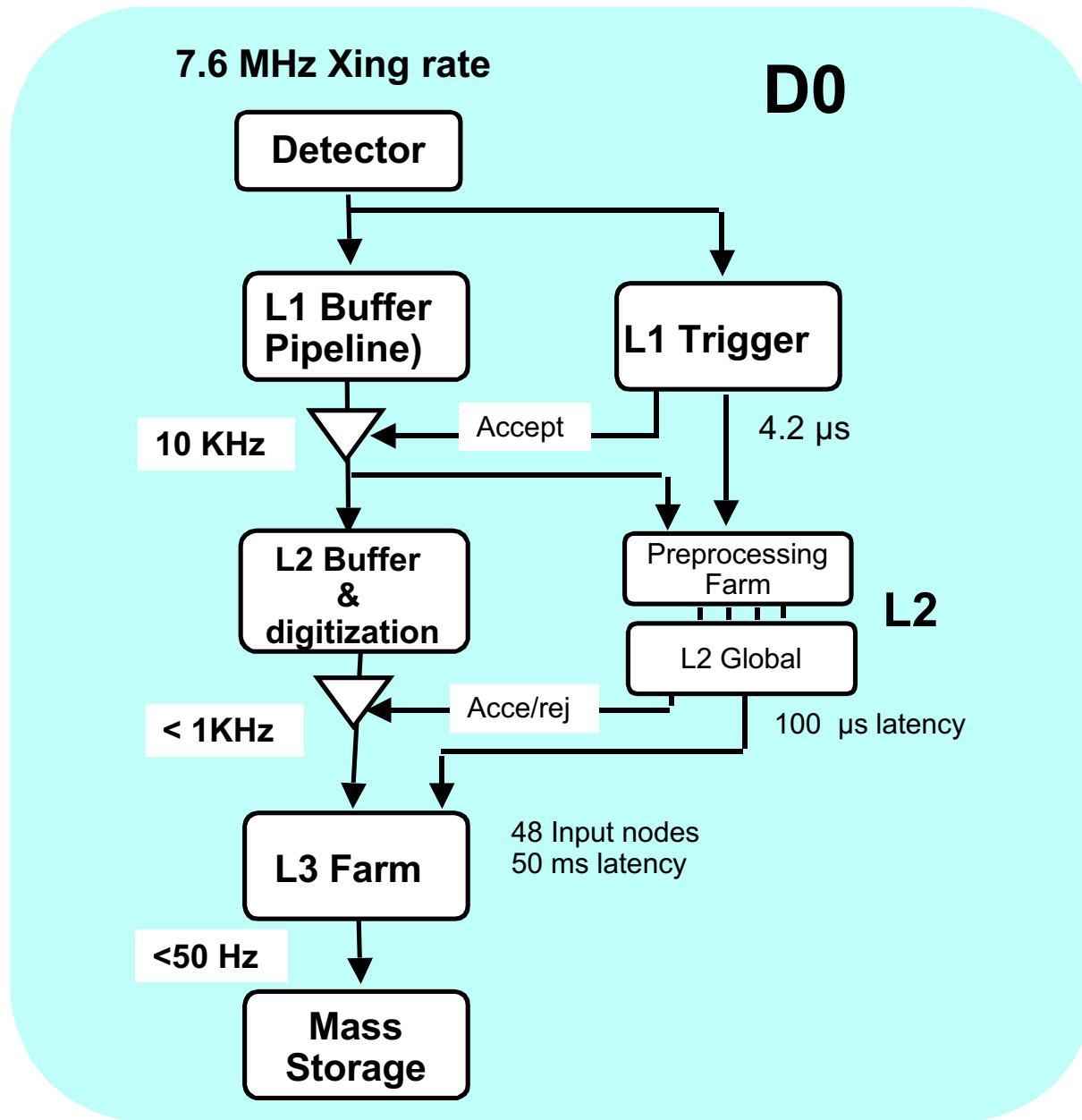


Can we achieve the ultimate T/DAQ system ?

Tevatron selection scheme

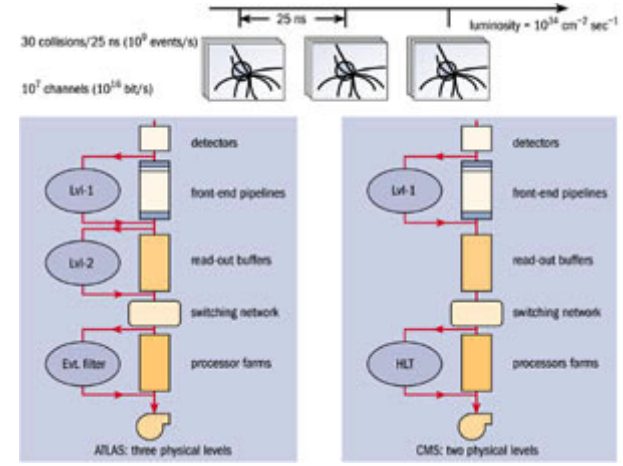
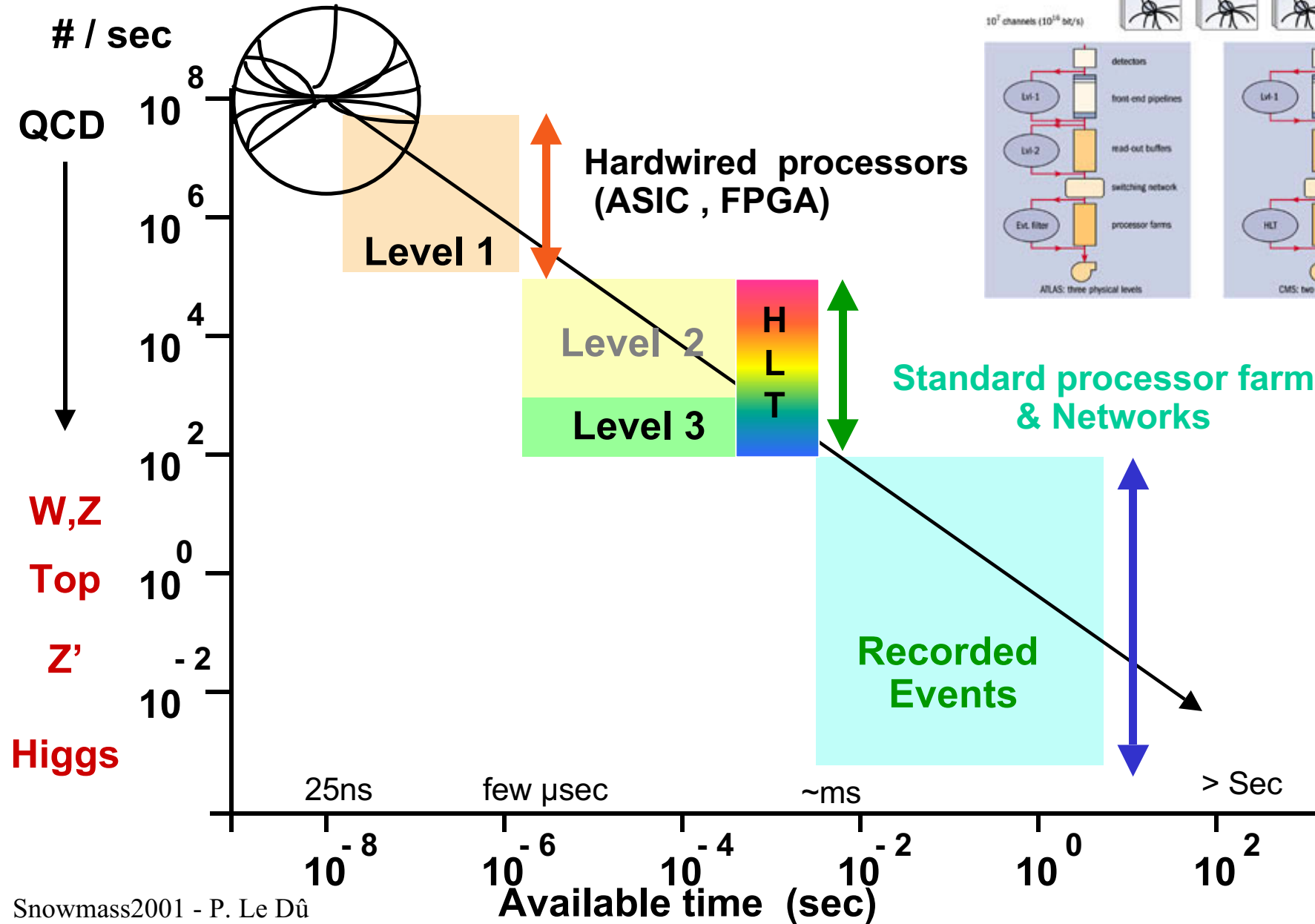
Production rate





LHC Multilevel Selection scheme

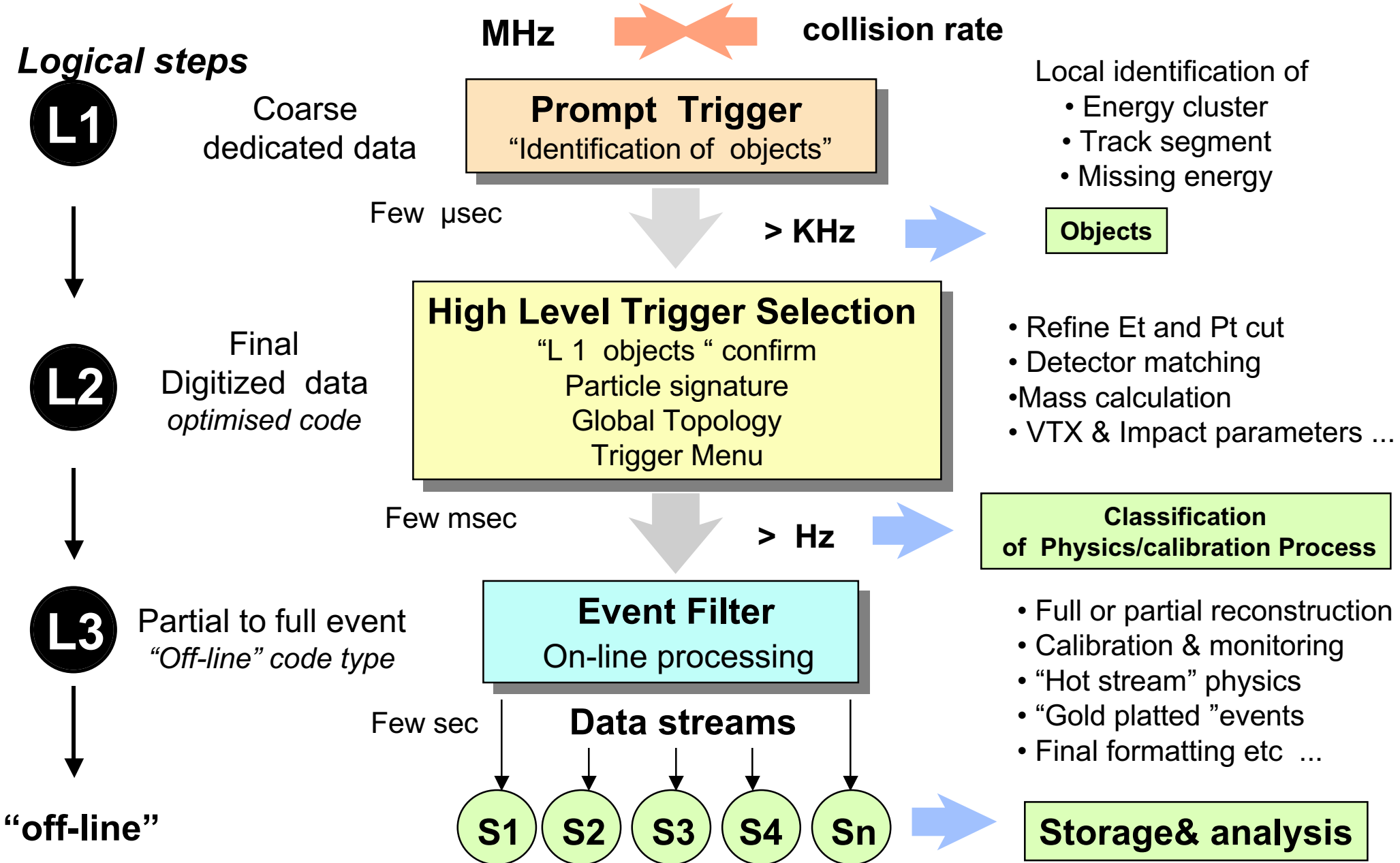
Production rate



Evolution → 2005-2010

- **LHC (ATLAS & CMS) → Two levels trigger**
 - L1 = physics objects (e/g,jet,m ..) using dedicated data
 - L2 + L3 = **High Levels** « software » Triggers using « digitized data »
- **Complex algorithms like displaced vertices are moving downstream**
 - CDF/DO : L2 vertex trigger
 - LHCb/Btev : L0/L1 b trigger
- **Use as much as possible commodity products (HLT)**
 - No more « Physic » busses → VME,PCI ..
 - Off the shelf technology
 - Processor farms
 - Networks switches (ATM, GbE)
 - Commonly OS and high level languages

“Logical Strategy” for event selection



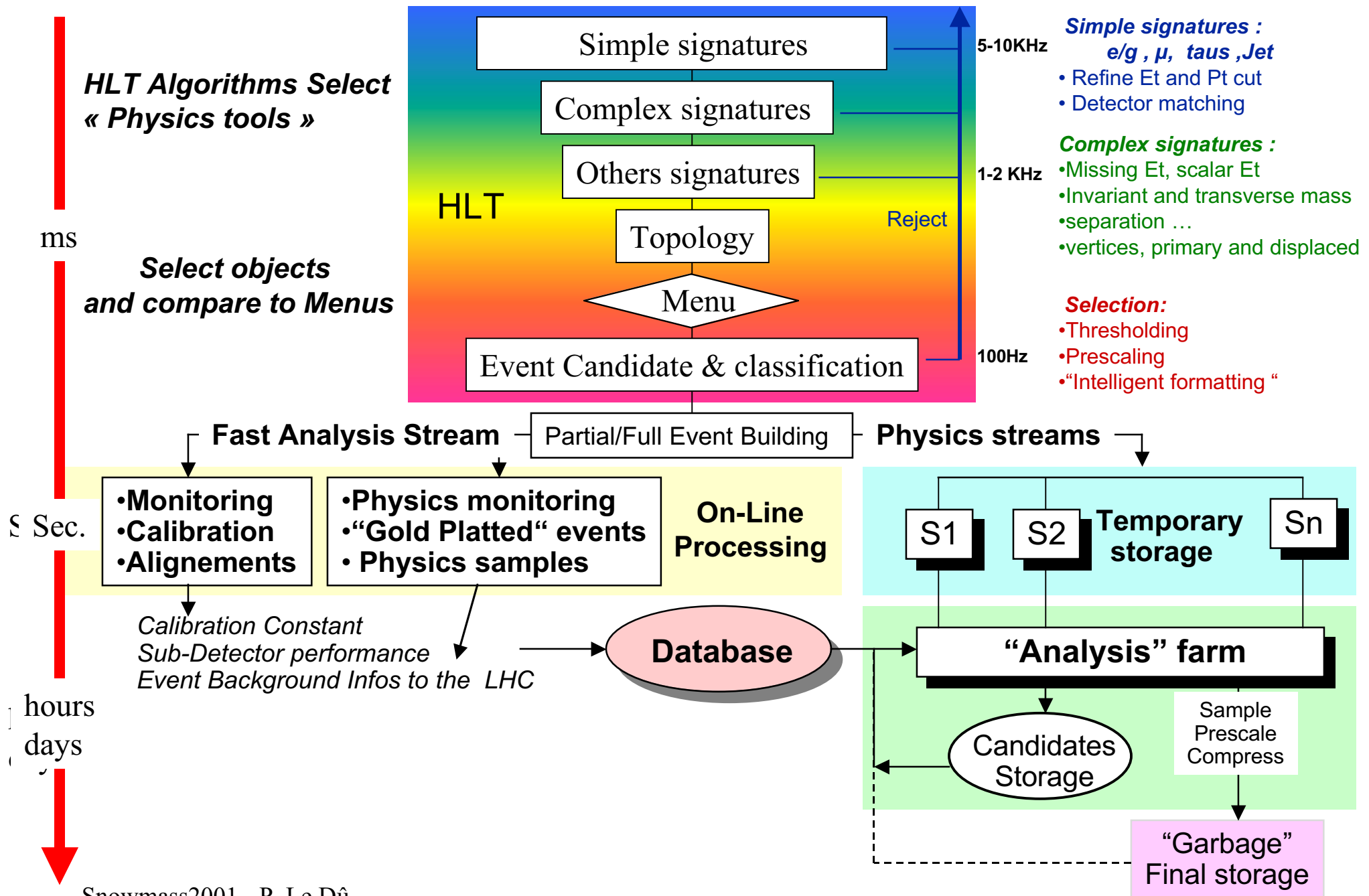
On-off line boundaries



become flexible

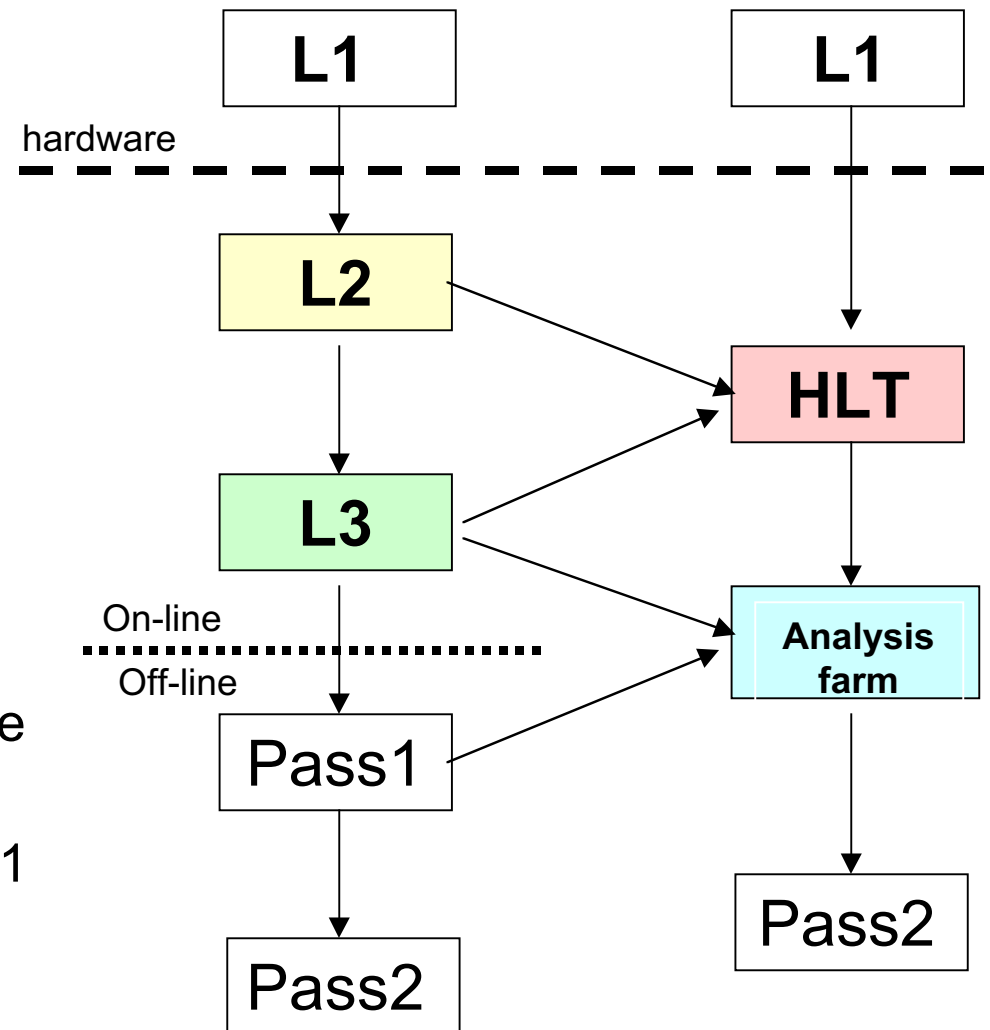
- Detectors are becoming more stable and less faulty
- On-line processing power is increasing and use similar hw/sw components (PC farms..)
- On-line calibration and correction of data possible
- More complex analysis is moving on-line
 - Filter event
 - Sort data streams...

Trigger strategy & Event Analysis



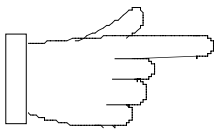
Summary of T/DAQ architecture evolution

- Today
 - Tree structure and partitions
 - Processing farms at very highest levels
 - Trigger and DAQ dataflow are merging
- Near future
 - Data and control networks centered
 - Processing farm already at L2
- More complex are moving on line
- Boundaries between on-line and off-line are flexible
- Commodity components more towards L1



What next ? 2010-2020

- **Next generation of machines**
 - LC (Tesla,NLC,JLC)
 - Concept of « **software trigger** »
 - VLHC : like LHC
 - CLIC : < ns sec collision time!
 - Mu collider : Not investigated yet!
- **Next generation of detectors :**
 - Pixels trackers : ex 800 M Ch (Tesla)
 - Si-W calorimeters: 32 M Ch. (Tesla)



Challenges

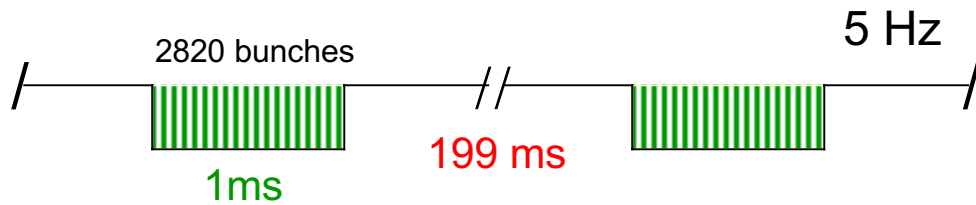
Very high luminosity $> 10^{34}$

High or continuous collision rate (< ns)

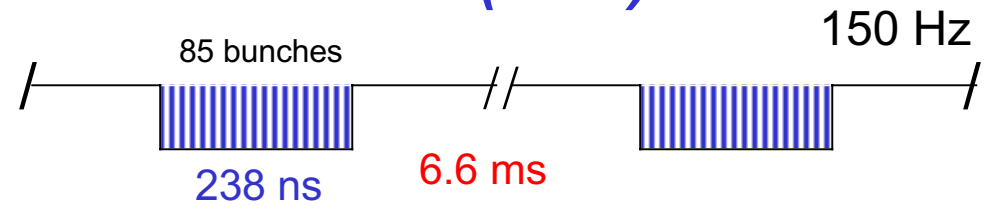
multimillion Si read-out channels

LC beam structure

TESLA



JLC (NLC)



- Relatively long time between bunch trains **199 ms**
- Rather long time between bunches: 337 ns
- Rather long bunch trains (same order as detector read-out time: **1ms**)

- Relatively long time between bunch trains (same order as read-out time): **6.6 ms**
- Very short time between bunches: 2.8 ns
- Rather short pulses : **238 ns**

LC basic trigger concept : **NO hardware trigger**

- **Read-out and store front end digitized data of a complete bunch train into buffers**
 - Deadtime free -- no data loss
- **DAQ triggered by every train crossing**
 - build the event and perform zero suppression and/or data compression
 - full event data information of complete bunch train available
- **Software selection between train : software trigger**
 - using « off-line » algorithms
- **Classify events according**
 - physics, calibration and machine needs
- **Store events :**
 - partial or everything!

Advantages

- **Flexible**
 - fully programmable
 - unforeseen backgrounds and physics rates easily accomodated
 - Machine people can adjust the beam using background events
- **Easy maintenance and cost effective**
 - Commodity products : Off the shelf technology (memory, switches, processors)
 - Commonly OS and high level languages
 - on-line computing ressources usable for « off-line »
- **Scalable :**
 - modular system

Consequences on detector concept

- **Constraints on detector read-out technology**
 - **TESLA: Read 1ms continuously**
 - VTX: digitizing during pulse to keep VTX occupancy small
 - TPC : no active gating
 - **JLC/NLC :**
 - **7 ms pulse separation**
 - detector read out in 5 ms
 - veto trains
 - **3 ns bunch separation**
 - off line bunch tagging
- **Efficient/cheap read-out of million of front end channels should be developed**
 - silicon detectors (VTX and SiWcalorimeters)

Conclusion about LC triggers

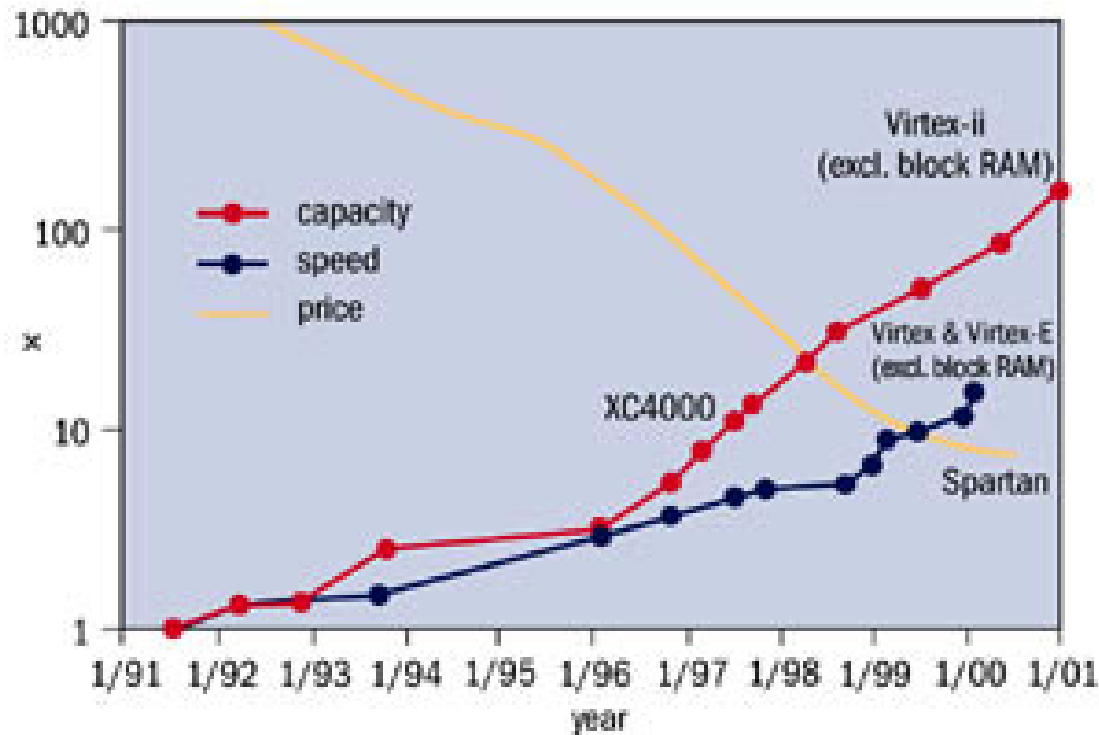
- **Software trigger concept remains the ‘ baseline ’**
 - T/DAQ for the LC is NOT an issue !
- **Looks like the ‘ ultimate trigger ’**
 - satisfy everybody : no loss and fully programmable
- **Feasible - (almost) today and affordable**
 - Less demanding than LHC
- **Consequence on the detector design**
 - constraint on detectors read-out electronics (trackers)
- **Consequence on the software environment:**
 - on and off-line are merging : need to develop a complete integrated computing model with common resources from calibration, selection (algorithms and filter) and analysis /processing paths....

Technology forecast (2005-2015)

Fast logic & hardware triggering (L1)



- **Move to digital & programmable**
- ASICs not anymore developed
- **FPGA's** is growing and can embed complex algorithms



Technology forecast (2005-2015) (Software trigger)

Systematic use of : Off the Shelves commodity products

- Processors and memories
 - Continuous increasing of the computing power
 - More's law still true until 2010! → x 64
 - Then double every 3years →
x 256 by 2016
 - Memory size quasi illimited !
 - Today: 64 Mbytes
 - 2004 : 256 MB
 - 2010 : > 1 GB
- Networks: Commercial telecom/computer standards
 - Multi (10-100) GBEthernet
 - But : Software overhead will limit the performance...

About standards

- **Evolution of standards : no more HEP!**
 - HEP : NIM (60s) CAMAC (70s), FASTBUS (80s),
 - Commercial OTS : VME (90s), PCI (2000) → CPCI?
- **Looking ahead: today commercial technologies**
 - No wide parallel data buses in crates
 - Backplanes used for power distribution, serial I/O, special functions
 - High speed Gb/s fiber & copper serial data links
 - Wireless data link emerging
 - Higher densities for micros, memories standards commercial part
 - Hundred of pin packages

Transfer to other fields

- **Last year IEEE NSS-MIC Conference shows a great interest and a common interest**
- **Medical Imaging as similar requirement as us for diagnostic TEP**
 - Large data movement and on-line treatment
 - Fast selection and reconstruction

Final Conclusions

- Trigger/should not be an issue for the next generation of machines like LCs
- Fully commercial OTS commodity components
- Programmable & software triggers
- On-line and Off-line boundaries become very flexible: need a new « computing model »
- Challenges for 2020
 - Very high luminosity $> 10^{34}$
 - High or continuous collision rate ($< ns$)